VLSI and Nanoelectronics (Chip Designing) Research Group of Dr. Sajad A Loan won three best paper awards.

It is a matter of great honor to the whole Jamia Millia Islamia that VLSI and Nanoelectronics (Chip designing) research group of Dr. Sajad A Loan of Electronics Engineering Department has won two best paper awards in the recently concluded IEEE Conference IMPACT-2017, conducted by Electronics Engineering Department AMU Aligarh, 24-26th of November, 2017. It is worth to mention that just last month (3-5th October, 2017) one more research paper of the same group won best paper award in IEEE IEMCON 2017 in the University of British Colombia, Vancouver, Canada, so three best paper awards in a month. It is a big achievement and we do hope that they bring more and more laurels to university in future to make it one of the best in India/world.

The details of the papers are given below.

Paper 1: Ashita, Sajad A. Loan, M. Rafat, "Investigation of leakage in a FinHBTFET with stack gate underlap" IEEE IMPACT-2017 AMU **(presented by Ms. Ashita Kumar, awarded in Device Modelling section)**

Paper 2. M. Nizammuddin, Sajad A Loan , "High performance CNT based folded cascode OTA"IEEE IMPACT-2017 AMU**(presented by Dr. M. Nizammuddin, awarded in Analog Signal Processing section)**

Paper 3, Ehteshyam, Sajad A Loan, M. Rafat,"A junctionless inverted TFETwith increased ON current and reduced ambipolarity" IEEE IEMCON-2017 UBC Canada. **(Presented by Dr. Sajad A Loan, awarded in VLSI and embedded section)**