Dr. S. Intekhab Amin

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Office Address	Department of Electronics & Communication Engineering, Faculty of Engineering & Technology, Jamia Millia Islamia, Jamia Nagar, New Delhi-110025.
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Area of Research

Device modeling, Design and Simulation of silicon and III-V based Semiconductor Devices viz. Junctionless MOSFET, TFET, FB-FET, TFT, Ferroelectric Devices, Device modeling for sensor application, Digital VLSI Circuits and System Design, Analog/RF Device, Circuits and Sub-system Design for neuromorphic application

Educational Qualification

Ph.D	VLSI and Nanoscale Semiconductor Devices from **National Institute of Technology Jalandhar,** Punjab, completed in Jan. 2017
M.Tech	Electronic Circuits & System Design from **Z.H.C.E.T, AMU** Aligarh, completed in Aug-2009
AMIE	Electronics & Communication Engineering **from The Institution of Engineers India**, completed in Jun-2006

Work Experience

March 2017-Till date: Assistance Professor, Department of Electronics & Communication Engineering, JMI

July 2010- Aug. 2012: Assistance Professor, Department of Electronics & Communication Engineering, MRCE Faridabad

Research Publications.

A. Journals

1. Aadil Anam, **S.Intekhab Amin** , Dinesh Prasad, "Novel III-V inverted T-channel TFET with dual-gate impact on line tunneling, with and without negative capacitance, Microelectronics Journal, Volume 151, 106309, September 2024, https://doi.org/10.1016/j.mejo.2024.106309 (SCI, IF=1.9)

2. Aadil Anam, **S.Intekhab Amin** , Dinesh Prasad, "Optimizing InGaAs/GaAsSb Staggered Bandgap U-Gate Line TFET With p^+-Pocket Implant and Negative Capacitance for Enhanced Performance," IEEE Transactions on Nanotechnology, Vol. 23, pp.584-590, Aug. 2024, DOI: 10.1109/TNANO.2024.3437669 (SCIE, IF=2.1)

3. Aadil Anam, **S.Intekhab Amin** , Dinesh Prasad "Raised Ge-Source with n^+ pocket and recessed drain line TFET: A proposal for biosensing applications," Materials Science and Engineering: B, Volume 306, 117456, August 2024, https://doi.org/10.1016/j.mseb.2024.117456, (SCI, IF=3.9)

4. Aadil Anam, **S.Intekhab Amin** , Dinesh Prasad, "III-V material-based junction-free L-shaped gate normal line tunneling FET for improved performance," *Semicond. Sci. Technol.* **39** 095004, Aug-2024, **DOI** 10.1088/1361-6641/ad689d (SCI, IF=1.9)

5. Nuzhat Yousf, Aadil Anam, Zuber Rasool, S. Intekhab Amin, "Ultralow-Power DST-TFET pH Sensor Exceeding the Nernst Limit with Influence of Temperature on Sensitivity," *ACS Applied Bio Materials*, Vol 7/Issue7, June 2024, DOI: 10.1021/acsabm.4c00428, (SCIE, IF=4.6)

6. Aadil Anam, **S.Intekhab Amin** , Dinesh Prasad, "Exploring Intertwined quantum and cryogenic behaviour in ultra-scaled 10 nm MOSFET: a NEGF quantum ballistic simulation," *Phys. Scr.* **99** 065931, May 2024, **DOI** 10.1088/1402-4896/ad41a3 (SCI, IF=2.6)

7. Leo Raj Solay, Naveen Kumar, Sarabdeep Singh, **S Intekhab Amin**, Saravanan Yuvaraja and Sunny Anand "Design and sensitivity analysis of GAA nanowire dopingless FET based label free biosensor," *Phys. Scr.* **99** 065040, May 2024, **DOI** 10.1088/1402-4896/ad4926, (SCI, IF=2.6)

8. Aadil Anam, **S.Intekhab Amin** , Dinesh Prasad, Naveen Kumar , Sunny Anand, "Effect of ambipolarity suppression in PNPN TFET with dopant segregated Schottky-drain technique," Microelectronics Journal, Volume 145, March 2024, 106116, https://doi.org/10.1016/j.mejo.2024.106116 (SCI, IF=1.9)

9. Bashir, I., **Amin, S.I**., Majeed, L. *et al*. "Comprehensive analysis of single and double gate organic phototransistor. *Opt Quant Electron* **55**, 1095 Sep. (2023). https://doi.org/10.1007/s11082-023-05350-2 (SCI, IF=3.3)

10. Aadil Anam, **S Intekhab Amin**, Dinesh Prasad, Naveen Kumar and Sunny Anand "Charge-plasma-based inverted T-shaped source-metal dual-line tunneling FET with improved performance at 0.5V operation," *Phys. Scr*. **98** 095918, Aug. 2023, **DOI** 10.1088/1402-4896/aceb95 (SCI, IF=2.6)

11. Aadil Anam, , **S Intekhab Amin**, Dinesh Prasad, Naveen Kumar and Sunny Anand, **"**Undoped vertical dual-bilayer TFET with a super-steep sub-threshold swing: proposal and performance comparative analysis," Semiconductor Science and Technology, Volume 38, Number 7, 2023, doi: 10.1088/1361-6641/acd2f9 (SCI, IF=1.9)

12. Aadil Anam, , **S Intekhab Amin**, Dinesh Prasad, Naveen Kumar and Sunny Anand, "Analysis of III-V material-based dual source T-channel junction-less TFET with metal implant for improved DC and RF performance**," Micro and Nanostructure, Volume 181, September 2023, 207629, https://doi.org/10.1016/j.micrna.2023.207629, (SCI, IF=3.1)**

13. Aadil Anam, Naveen Kumar, **S Intekhab Amin**, Dinesh Prasad and Sunny Anand, "Charge-plasma based symmetrical-gate complementary electron–hole bilayer TFET with improved performance for sub-0.5 V operation," *Semicond. Sci. Technol.* **38** 015012, 2023, **DOI** 10.1088/1361-6641/aca7db, (**SCI, IF=2.04**)

14. Majeed, Lubna, **Syed Intekhab Amin**, Zuber Rasool, Ishrat Bashir, Naveen Kumar, and Sunny Anand. 2023. "TCAD Device Modeling and Simulation Study of Organic Field Effect Transistor-Based pH Sensor with Tunable Sensitivity for Surpassing Nernst Limit" *Electronics* 12, no. 3: 536. https://doi.org/10.3390/electronics12030536, (**SCI, IF=2.69**)

15. Rasool, Z., **Amin, S.I**., Majeed, L. *et al*. Simulation-based Study of Super-Nernstian pH Sensor Based on Doping-less Tunnel-field Effect Transistor. *Silicon* (2023). https://doi.org/10.1007/s12633-023-02329-2 (**SCI, IF=2.94**)

16. Solay, Leo Raj, Kumar, Pradeep, **Amin, S Intekhab**, Anand, Sunny, "Investigation of Common Source Amplifier Circuit using Gate Stack-Based GAA Dopingless Nanowire Field Effect Transistor," ECS Journal of Solid State Science and Technology, Volume 11, Number 8, Aug. 2022. (**SCI, IF=2.07**)

17. Solay, Leo Raj, Kumar, Naveen, **Amin, S Intekhab**, Kumar, Pradeep, Anand, Sunny, "Design and performance analysis of gate-all-around negative capacitance dopingless nanowire tunnel field effect transistor," 2022, ***Semicond. Sci. Technol***. 37 115001. **(SCI, IF=2.04)**

18. M. Y. Iqbal, M. S. Alam, S. Anand and **S. I. Amin**, "A FoM for Investigation of SB TFET Biosensor Considering Non-Ideality," in ***IEEE Transactions on***

***Nanotechnology*,** vol. 21, pp. 251-258, 2022, doi: 10.1109/TNANO.2022.3178845. (**SCI, IF=2.96**)

19. Mohammad Shoaib, **S. Intekhab Amin**, Naveen Kumar, Sunny Anand, Ankush Chunn and M. Shah Alam, "Device and Circuit Level Assessment of Negative Capacitance TFETs for Low-Power High-Performance Digital Circuits," ***ECS J. Solid State Sci. Technol.*** Vol. **11,** p-053011, May.2022, (**SCI, IF=2.07**)

20. Mohd Anas, **S. Intekhab Amin**, Mirza Tariq Beg, Aadil Anam, Ankush Chunn & Sunny Anand, "Design and Analysis of GaSb/Si Based Negative Capacitance TFET at the Device and Circuit Level," **Springer, *Silicon*** (2022). https://doi.org/10.1007/s12633-022-01918-x, (**SCI, IF=2.67**)

21. Kritika Lal, Anushka Verma, Pradeep Kumar, Naveen Kumar, S. Intekhab Amin & Sunny Anand, "Design and Performance Enhancement of Gate-on-Source PNPN Doping–Less Vertical Nanowire TFET," **Springer, *Silicon***, **14**, pages 4375–4382 (2022), (**SCI, IF=2.67**)

22. Mohd Ashraf Lone, Leo Raj Solay, Amandeep Singh, S. Intekhab Amin & Sunny Anand, "Design and Implementation of Negative Capacitance Based Electrostatic Doped Double Gate Tunnel Field Effect Transistor," **Springer, *Silicon*** (2022). https://doi.org/10.1007/s12633-022-01932-z, (**SCI, IF=2.67**)

23. Anjana Bhardwaj, Leo Raj Solay, Naveen Kumar, S. Intekhab Amin, Amandeep Singh, Balwinder Raj, Pradeep Kumar & Sunny Anand, "Doping-less TFET Based Common Source Amplifier Implementation and Behaviour Analysis Under Symmetric and Asymmetric Conditions," **Springer, *Silicon*** (2022). https://doi.org/10.1007/s12633-022-01921-2, (**SCI, IF=2.67**)

24. Leo Raj Soley, **S. Intekhab Amin**, Pradeep Kumar, Sunny Anand, **"**Enhancing the design and performance of a gate-all-around (GAA) charge plasma nanowire field-effect transistor with the help of the negative-capacitance technique," ***J Comput Electron*, (2021)**, **Springer,** https://doi.org/10.1007/s10825-021-01808-2, (**SCI, IF=1.807**)

25. Himanshu Bhradwaj, Naveen Kumar, **S. Intekhab Amin**, Sunny Anand, "Charge Plasma Based Vertical Nanowire Tunnel Field Effect Transistor: Design and Sensitivity Analysis for Biosensing Application," **Springer, *Silicon, Nov***. 2021. https://doi.org/10.1007/s12633-021-01512-7, (**SCI, IF=2.67**)

26. Kosheen Wighmal, Giridhar Peddi, Apoorva, Naveen Kumar, **S. Intekhab Amin,** Sunny Anand, **"**Gate All Around Dopingless Nanotube TFET Biosensor with Si0.5Ge0.5 Based Source**," Springer, *Silicon*, Sep. 2021,** https://doi.org/10.1007/s12633-021-01361-4 (**SCI, IF=2.67**)

27. Manish Kumar Singh, **Syed Intekhab Amin** and Amit Choudhary, "A survey on the characterization parameters and lifetime improvement techniques of wireless sensor network," ***Frequenz*,** vol. 75, no. 9-10, pp. 431-448, Aug. 2021, (**SCIE, IF=0.726**)

28. Kritika Lal, Anushka Verma, Pradeep Kumar, Naveen Kumar, **S. Intekhab Amin**, Sunny Anand, "Design and Performance Enhancement of Gate-on-Source PNPN Doping–Less Vertical Nanowire TFET," **Springer,** ***Silicon*** (2021). https://doi.org/10.1007/s12633-021-01222-0, **(SCI, IF=2.67**)
29. Archika singh, Mumin Sajad, Amandeep Singh, Naveen Kumar, **S. Intekhab Amin**, Sunny Anand, **"**Design and analysis of negative capacitance based dual material dopingless tunnel FET**," Elsevier, Superlattices and Microstructures,** Volume 156, Aug. 2021, 106964, https://doi.org/10.1016/j.spmi.2021.106964, (**SCI, IF=2.658**)

30. Apoorva, Naveen Kumar, **S. Intekhab Amin**, Sunny Anand**,** Design and investigation of negative capacitance–based core-shell dopingless nanotube tunnel field-effect transistor, **IET Circuit Device & Syst**., 21 March 2021, 1-9, https://doi.org/10.1049/cds2.12064 (**SCI, IF=1.29**).

31. Manish Kumar Singh, **Syed Intekhab Amin**, Amit Choudhary, **"**Genetic algorithm based sink mobility for energy efficient data routing in wireless sensor networks," **AEU-International Journal of Electronics and Communications**, Volume 131, March 2021, 153605, https://doi.org/10.1016/j.aeue.2021.153605, (**SCI IF=3.18**)

32. Leo Raj Soley, Sarabdeep Singh, Naveen Kumar, **S. Intekhab Amin**, Sunny Anand "Design of Dual-Gate P-type IMOS Based Industrial Purpose Pressure Sensor," **Springer,** ***Silicon*** **(2020), Oct. 2020 DOI:10.1007/s12633-020-00785-8** (**SCI, IF=1.499**)

33. Amrita Singh, **S. Intekhab Amin,** Sunny Anand, "Label Free Detection of Biomolecules Using SiGe Sourced Dual Electrode Doping-Less Dielectrically Modulated Tunnel FET," **Springer,** ***Silicon*** **(2020), Jan. 2020** DOI: 10.1007/s12633-019-00325-z (**SCI, IF=1.499**)

34. Umer Mushtaq, Naveen Kumar, Sunny Anand, **S. Intekhab Amin**, "Design and Performance Analysis of Core-Shell Dual Metal-Dual Gate Cylindrical GAA Silicon Nanotube-TFET," **Springer,** ***Silicon*** **(2020), DOI: 10.1007/s12633-019-00329-9** (**SCI, IF=1.499**)

35. Simran Kaur, R.K. Sarin, Sunny Anand, and **S. Intekhab Amin,** "6-T and 7-T SRAM CELL Design Using Doping-Less Charge Plasma TFET,"**Springer,** ***Silicon*** **(2020).** https://doi.org/10.1007/s12633-020-00713-w (**SCI, IF=1.499**)

36. Manish Kumar Singh, **S. Intekhab Amin,** "Energy efficient wireless sensor network using optimum hops and virtual MIMO technique," **SN Applied Sciences (2020)** 2:1582 Aug. 2020| https://doi.org/10.1007/s42452-020-03360-3, (SCOPUS index)

37. Adil Anam, Sunny Anand, **S. Intekhab Amin,** "Design and Performance Analysis of Tunnel Field Effect Transistor with Buried Strained $Si_{1-x}Ge_x$Source Structure Based Biosensor for Sensitivity Enhancement," **IEEE Sensors**

Journal, Volume: 20 , Issue: 22 , Jun. 2020, pp. 13178 – 13185, doi: 10.1109/JSEN.2020.3004050, (**SCI, IF=3.07**)

38. Amrita Singh, **S. Intekhab Amin**, Sunny Anand, "Implementation of negative capacitance over SiGe sourced Doping-less Tunnel FET," **Elsevier, Superlattice & Microstructures,** Vol. 145, September 2020, p. 106580, DOI: https://doi.org/10.1016/j.spmi.2020.106580 (**SCI, IF=2.12**)

39. Manish Kumar Singh, **S. Intekhab Amin,** "Energy-efficient data transmission technique for wireless sensor networks based on DSC and virtual MIMO," **ETRI Journal, Wiley,** Vol. 42, pp.341–350 April 2020, **https://doi.org/10.4218/etrij.2018-0632** (**SCI, IF=1.09**)

40. Apoorva, Naveen Kumar, **S. Intekhab Amin**, Sunny Anand, "Design and Performance Optimization of Novel Core-Shell Dopingless GAA-Nanotube TFET with Si0.5Ge0.5 Based Source," **IEEE Tran. Electron Device**, vol. 67, no.3, pp. 789-795, March. 2020, DOI-10.1109/TED.2020.2965244. (**SCI, IF=2.7**)

41. Shruti Shrey, Naveen Kumar, Sunny Anand, and **Intekhab Amin**, "Performance Analysis of a Charge Plasma Junctionless Nanotube Tunnel FET Including the Negative Capacitance Effect," **Journal of Electronic Materials, Springer,** vol. **49, pp.** 2349–2357, Jan. 2020, https://doi.org/10.1007/s11664-020-07969-3. (**SCI, IF=1.67**)

42. Amrita Singh, **S. Intekhab Amin,** Sunny Anand, , "Label Free Detection of Biomolecules Using SiGe Sourced Dual Electrode Doping-Less Dielectrically Modulated Tunnel FET," **Springer, Silicon**, vol. 12**,** pp. 2301–2308 , Jan. 2020, https://doi.org/10.1007/s12633-019-00325-z, (**SCI, IF=1.21**).

43. Lubna Gajal, Naveen Kumar, Sunny Anand and **S. Intekhab Amin**, "Design and Performance Enhancement of Doping-less Field Effect Transistor with the help of Negative Capacitance Technique, Springer," **Springer, Applied Physics A**, Vol. 126, p. 45 Dec. 2019, DOI: 10.1007/s00339-019-3229-x. (**SCI, IF=1.76**)

44. Umar Mushtaq, Naveen Kumar, Sunny Anand and **S. Intekhab Amin,** "Design and Performance Analysis of Core-Shell Dual Metal-Dual Gate Cylindrical GAA Silicon Nanotube-TFET," **Springer, Silicon Journal**, vol. 12, pp. 2355–2363 Dec. 2019. https://doi.org/10.1007/s12633-019-00329-9. (**SCI, IF=1.21**)

45. Shruti Shreya, Adnan Hamid Khan, Naveen Kumar, **S. Intekhab Amin**, Sunny Anand, "Core-Shell Junctionless Nanotube Tunnel Field Effect Transistor: Design and Sensitivity Analysis for Biosensing Application," **IEEE Sensor Journal,** vol. 20, pp. 672 – 679, Oct. 2019 **DOI:** 10.1109/JSEN.2019.2944885. (**SCI, IF=3.07**)

46. Sunny Anand, Amrita Singh, **S. Intekhab Amin**, Asmita Thool, "Design and Performance Analysis of Dielectrically Modulated Doping-less Tunnel FET

based label free Biosensor," **IEEE Sensor Journal**, Vol. 19, pp. 4369 – 4374, Feb. 2019 (**SCI, IF=3.07**).

47. **S. Intekhab Amin**, Lubna Gajal, and Sunny Anand, "Analysis of Dielectrically Modulated Doping-less Transistor for Biomolecules Detection by using the Charge Plasma Technique**, Springer, Applied Physics A**, pp.578-585, Aug. 2018, DOI: 10.1007/s00339-018-2003-9, (**SCI, IF=1.604**)

48. Naveen Kumar, Umar Mushtaq, **S Intekhab Amin**, Sunny Anand, "Design and Performance Analysis of Dual- Gate All around Core Shell Nanotube TFET," **Elsevier, Superlattice and Microstructure**, Vol. 125, pp. 356-354, Jan. 2019, https://doi.org/10.1016/j.spmi.2018.09.012. (**SCI, IF=2.09**)

49. Leo Raj Soley, Sarabdeep Singh, **S. Intekhab Amin**, Sunny Anand, "Design and Analysis of Gate Engineered Dual Material Gate Double Gate Impact Ionization Metal Oxide Semiconductor," **Transaction on Electrical and Electronic Material, Springer,** Nov. 2018, DOI https://doi.org/10.1007/s42341-018-0080-2, (**SCI, IF=1.9**)

50. Suman Kumar Meena, Asmita Thool, R.K. Sarin, **S. Intekhab Amin**, Sunny Anand, "An Analytical Model for Potential and Electric Field Distribution of Dual Electrode Doping Less Tunnel Field Effect Transistor," Material Focus, Vol. 7, no. 2, pp.1-7, May 2018.

51. Syed Afzal Ahmad, Naushad Alam, **S. Intekhab Amin**, "Impact of Pocket-Size Variation on the Performance of GaAs0.1Sb0.9/InAs based Heterojunction Double Gate TFET," **Journal of Nanoelectronics and Optoelectronics, Volume 13, Number 7, July 2018, pp. 1009-1018(10)**, https://doi.org/10.1166/jno.2018.2335 ,(**SCI, IF=0.497**).

52. Umar Mir, Leo, **S. Intekhab Amin,** Sunny Anand, "Design and Analog performance Analysis of Triple Material Gate based Doping less-Tunnel FET," **Journal of Nanoelectronics and Optoelectronics, Volume 14, Number 8, August 2019, pp. 1177-1182(6)**, https://doi.org/10.1166/jno.2019.2662 (**SCI, IF=0.497**).

53. Sk. Safiul Baksh, R. K. Sarin, **S. Intekhab Amin**, and Sunny Anand, "Design of GaAs based Junctionless Field Effect Transistor and its Performance Evaluations," **ASP**, **Journal of Nanoelectronics and Optoelectronics, Volume 13, Number 1, January 2018, pp. 32-37(6),** https://doi.org/10.1166/jno.2018.2171 (**SCI, IF=0.497**).

54. Gurmeet Singh, **S.Intekhab Amin**, Sunny Anand, and R. K. Sarin, "Design of $Si_{0.5}Ge_{0.5}$ Based Tunnel Field Effect Transistor and its Performance Evaluation," **Superlattice and Microstructure, Elsevier**, vol. 92, pp. 143-156, Apr. 2016, (**SCI, IF=2.09**), https://doi.org/10.1016/j.spmi.2016.02.027.

55. **S. Intekhab. Amin**, and R.K. Sarin, "Enhanced Analog Performance of Charge Plasma Based Dual Material and Gate Stacked Architecture of Junctionless

Transistor With High-k Spacer," **Applied Physics A, Springer,** vol. 122, pp.380-389, Mar. 2016, https://doi.org/10.1007/s00339-016-9904-2, (**SCI, IF=1.604**)

56. Sunny Anand, **S Intekhab Amin**, and R.K.Sarin, **"**Performance analysis of charge plasma based Dual Electrode Tunnel FET," **J. of Semiconductors, IOP Science,** vol.37, issue 3, Mar. 2016, Indexed in Scopus.

57. Sunny Anand, **S Intekhab Amin**, and R.K.Sarin, "Analog Performance Investigation of Charge Plasma Based Dual Electrode Tunnel FET." **J. of Comput. Electron., Springer,** vol. 15, issue 1, pp. 94-103, Mar. 2016, https://doi.org/10.1007/s10825-015-0771-4 , (**SCI, IF=1.43**).

58. **S. Intekhab Amin** and R.K.Sarin, "Direct Tunneling Gate Current Model for Symmetric Double Gate Junctionless Transistor With SiO_2/ High-k Gate stacked Dielectric**," J. of Semicond**., **IOP science**, vol.37, issue 2, pp. 34001-34005, Feb. 2016, ISSN online 1674-4926. Indexed in Scopus-Elsevier

59. **S. Intekhab. Amin**, and R.K. Sarin, "Charge-Plasma Based Dual-Material and Gate-Stacked Architecture of Junctionless Transistor for Enhanced Analog Performance," **Superlattices and Microstructures**, **Elsevier,** vol. 88, pp. 582-590, Oct. 2015, https://doi.org/10.1016/j.spmi.2015.10.017, (**SCI, IF=2.09**)

60. **S. Intekhab Amin** and R.K.Sarin, "The Impact of Gate Misalignment on Analog Performance of Dual-Material Double Gate Junctionless Transistor," **J. of Semiconductors, IOP science**, vol. 36, issue. 9, pp. 094001-094007, Sep. 2015, ISSN online 1674-4926. Indexed in Scopus-Elsevier, 10.1088/1674-4926/36/9/094001

61. **S. Intekhab Amin** and R.K.Sarin, "Analog Performance Investigation of Gate misaligned Double gate Junctionless Transistor," **J. of Computational Electronics**, **Springer**, vol. 14, Issue 3, pp 675-685, Sep. 2015, https://doi.org/10.1007/s10825-015-0705-1 (**SCI, IF=1.43**).

B. Conferences

1. Aadil Anam; S. Intekhab Amin; Dinesh Prasad, "Performance Analysis of InSb Source-Based Heterojunctionless Nanowire TFET for Low-Power Application: Design and Simulation," IEEE International Conference on Interdisciplinary Approaches in Technology and Management for Social Innovation (IATMSI), 14-16 March 2024, Gwalior, DOI: 10.1109/IATMSI60426.2024.10502440

2. Aadil Anam; S. Intekhab Amin; Dinesh Prasad "InSb Source-Based Heterojunctionless Nanowire Tunneling FET for Biosensing Application: Design and Analysis," IEEE International Conference on Interdisciplinary Approaches in

Technology and Management for Social Innovation (IATMSI), 14-16 March 2024, Gwalior, DOI: 10.1109/IATMSI60426.2024.10502773

3. Aadil Anam; S. Intekhab Amin; Dinesh Prasad, "Temperature Sensitivity and Reliability Study of Symmetrical U-Shaped Gate Line TFET: RF/Analog and Linearity Performance Analysis," IEEE International Symposium on Smart Electronic Systems (iSES), 18-20 December 2023, Ahmedabad, https://doi.org/10.1109/iSES58672.2023.00030

4. A. Adlakha, W. Hussain, L. R. Solay**, S. Intekhab Amin**, S. Anand and P. Kumar, "Design and Analysis of 6T SRAM Implementation upon Dual Gate Junctionless FET," *2023 3rd International Conference on Intelligent Technologies (CONIT)*, Hubli, India, 2023, pp. 1-6, doi: 10.1109/CONIT59222.2023.10205575.

5. Aadil Anam; S. Intekhab Amin; Dinesh Prasad, "Simulation study and comparative analysis of proposed novel hybrid DG-TFET with conventional TFETs structures for improved performance," *2021 IEEE International Symposium on Smart Electronic Systems (iSES)*, 2021, pp. 311-315, doi: 10.1109/iSES52644.2021.00079.

6. Leo Raj Solay; Pradeep Kumar; **Intekhab Amin;** Sunny Anand, Design and Analysis of Gate Engineered Gate-AII-Around (GAA) Charge Plasma Nanowire Field Effect Transistor, Conference: 2021 6th International Conference for Convergence in Technology (I2CT), 2-4 Apr., 2021 DOI: 10.1109/I2CT51068.2021.9417999

7. Aditya Mudgal, Anu Mehra, **S. Intekhab Amin** "Effect Of Dielectric Pocket on TFET at Source/Channel Junction in Buried SiGe Strained Source," IEEE International Conference on Communication and Signal Processing (ICCSP July 2020, DOI: 10.1109/ICCSP48568.2020.9182188

8. Manish Kumar Singh, **S. Intekhab Amin,** Vibhav Sachan, Amit Chaudhary, "Improving Energy- Efficiency in Wireless Sensor Network Using Cooperative MIMO Technique Based on SM," IEEE 2nd International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), 2018, DOI: 10.1109/ICMETE.2018.00040

9. Sunny Anand, **S. Intekhab Amin**, and R.K.Sarin, "Performance Analysis of Different Material Based Dual Electrode Doping-less TFET," in Europian Advanced Material Congress Sweden, 24-27 Aug. 2016, Volume 2, Issue 6, Page 384-387, Jun. 2017, ISSN : 2002-4428.

10. **S. Intekhab. Amin**, Sunny Anand, and R.K. Sarin, "Performance Investigation of Charge Plasma Based Dual Material Gate Junctionless Transistor," IEEE conf. UPCON 2016, IIT BHU, pp. 167-172, Dec. 2016.

11. **S. Intekhab Amin** and R.K.Sarin, "Junctionless Transistor: A review" CIIT 2013 Mumbai, IET Dig. Lib., pp. 432-439, 18-19 Oct.2013.

12. **S.Intekhab Amin** and M.Shah Alam, "Use of TCAD Tool for the fabrication of sub-40nm bulk MOSFET and its performance investigation", National conference on VLSI,MEMS and NEMS, VMN 2010, 23-24 Sept. 2010.

Resource Person/Invited Talk:

1. "Novel Nano-scale Transistors for the future VLSI applications," on 22-06-2023 in A three Day FDP on "VLSI Design and Development from 22-24 June 2023, NSRIT.
2. "VLSI Breakthrough," on 1st Sep-2024, IEEE Circuits and Systems Society Students Branch Chapters JMI, on 2 days workshop on VLSI 2024.

Research Grant: Project Grant of 10 Lacs under BSR Start-Up Sanctioned by UGC
Status: Completed
Title: Design Considerations and Performance Assessment of Tunnel FET based Dielectrically Modulated Biosensor Device

Training Undergone:

- TWO -WEEK INTERDISCIPLINARY REFRESHER COURSE in "ADVANCED RESEARCH METHODOLOGY

- Precipitated in **Two Week Online Refresher Course "ARTIFICIAL INTELLIGENCE" from 23-05-2022 to 04-06-20222 through online mode,**

- Precipitated in the 1-week ATAL Faculty Development Program (FDP) on "Application of Computers in Biology," from 07-06 to 11-06, 2021.

- Precipitated in the 1-week Faculty Development Program (FDP) on "VLSI Chip Design Hands-on using open source EDA," held from 08- to 12 July 2019.

- Precipitated in 7th two-week Refresher Course in Basic Science (Interdisciplinary) organized by UGC-HRDC, JMI, New Delhi during 5th Nov. to 19th Nov. 2019

- Precipitated in the 1-month "Orientation Program" held at UGC-Human Resource Development Center, JMI, New Delhi during 20th Feb. to 28th March 2018.

M.Tech Project Guided

S.no	Year	Student Name	Title	University
1	2024	NUZHAT YOUSF	Dual Source Mono-Gate Vertical Tunnel Field Effect Transistors: pH Sensing Application & Negative Capacitance Implementation	JMI
2	2023	Mohd. Sadique	**Study and Simulation of Fin-Field Effect Diode (Fin-FED)**	JMI
3	2023	Rahul	**Study and Modelling of Junction less Fin Field Effect Transistor (JL FinFET) VDTA based Oscillator**	JMI
4	2023	Lakhan Mehra	III-V Material Based Junctionless Vertical TFET And III-V Material Based Junctionless Vertical TFET Biosensor	JMI
5	2022	Ishrat Bashir	**DESIGN HIGHLY PHOTOSENSITIVE ORGANIC PHOTOTRANSISTOR FOR CMOS IMAGE PIXEL SENSOR**	JMI
6	2022	Lubna Majeed	**ORGANIC FIELD EFFECT TRANSISTOR BASED pH SENSOR**	JMI
7	2022	Zuber Rasool	**Study of Doping less Tunnel field effect Transistor (TFET) based pH Sensors**	JMI
8	2021	Javaid Ahmad Rather	Modeling and Simulation of organic TFT	JMI
9	2021	Md Zafar Alam	Design and investigation of Schottky Barrier based β-Ga2O3 Power MOSFET	JMI
10	2020	Mohammad Shoaib	Device and Circuit Level Assessment of Negative Capacitance TFETs for Low Power High-Performance Digital Circuit Application	JMI

11	2020	Arshid Ahmad Bhat	Analog and Radio Frequency Performance of Dopant Segragated SB MOSFET	JMI
12	2020	Mohd Anas	Design and Performance Analysis of GaSb/Si NC Tunnel-FET based Inverter and Ring Oscillator for Low power Applications	JMI
13	2020	Mohammad Hashim	Performance Analysis of Negative Capacitance TFETs for 6T SRAM Cell	JMI
14	2019	Waqar Ahmad Ahanger	Modeling of Heterojunction TFET for Dielectric Modulated Biosensor Applications	JMI
15	2019	Aadil Anam	Tunnel Field Effect Transistor based Biosensor	JMI

Ph.D Guided: 01

Name of Scholar	**Ph.D Title**	**Department**	**Supervisor/Co-supervisor**	**Status**
Manish Kumar Singh	Design and Analysis of Energy-Efficient Data Transmission Scheme for Wireless Sensor Network	Dept. of ECE, JMI	Supervisor	Completed
Ph.D Ongoing: 04				
Aadil Anam	Modeling and Simulation of Novel Nano-Transistors	Dept. of ECE, JMI	Supervisor	Ongoing
Zafar Alam	Design and Modeling of Power MOSFETs	Dept. of ECE, JMI	Co-Supervisor	Ongoing
Zuber Rasool	Novel Semiconductor Devices for Synaptic Neural Network	Dept. of ECE, JMI	Supervisor	Ongoing
Shyam Kishor Ranjan	Nanosheet FET based Devices and Its applications in Analog Signal Processing	Dept. of ECE, JMI	Co-Supervisor	Ongoing

Administrative Responsibilities at JMI

- Assistant DSW for the period of 2024-25
- President Football Club at Games and Sports JMI for 2024-26
- Sports Manager FET (Badminton) for Inter faculty Badminton Tournament held on 10-12 March 2023
- Department Sports coordinator for FET Sports FEST held on 24-26 Feb 2023
- Member to the Faculty Committee, F/o Engg., & Tech., from 09-02-2022 to 08-02-2025
- Verification Officer at Department and Faculty level Admission committee in 2021-22
- Member, Accreditation & Data Committee from Aug. 2021- till date
- Criteria In-charge NAAC 2021
- Time Table Incharge 2021 till date
- DRC member from 24-Nov. 2020 till date
- Coordinator Constitutional day celebration on 26th Nov. 2019
- Subject Association Advisor for Academic session 2019-2020 Dept. of ECE
- Assistant Superintendent for BE Exam 2019
- Coordinator, Seminar B.Tech during 2018-19
- Coordinator, Seminar B.Tech during 2017-18
- Coordinator, Major Project B.Tech during 2017-18
- Member Editorial Board, Departmental Magazine, SPECTRONICS, 2018

Subject Taught at UG and PG Level:

- Low Power VLSI
- Active Filter and Signal Processing
- Digital Circuits and System
- Analog Electronics
- Advanced Signal Processing
- Embedded System Design

Lab Conducted/Conducting:

- Logic Design
- Microwave
- Instrumentation

- Circuit Simulation

Seminar/Workshop:-

Attended

- Emerging Trend of Research in Electronics and Communication
- Electronics and Communication System Design Aspects, May 2015
- INUP Familiarization Workshop Nanofabrication Technology
- Recent Trends in Instrumentation and Control Engineering

Award and Recognition

- Editorial Board Member in Discover Nano, Springer, from April-2024
- Topic Advisor at Micromachines MDPI from Nov. 2022
- Volunteer Reviewer panel, MDPI
- Session Chair in ICNOC 2022
- Session Chair in JTACON-2020
- Reviewer IEEE Transaction Electron Devices
- Reviewer IEEE Transaction Nanotechnology
- Reviewer IEEE Sensor Journal
- Reviewer Journal of Nano and Opto Electronics.
- Reviewer Springer Silicon, J. of Compt. El.
- Held All India rank 2nd in section examination of IE (India)
- S N Ghosh memorial prize and Institution prize IE (India)
- Qualified GATE in 2007

Software Skills

Electronic Design Package : Silvaco TCAD TOOL,ADS, Xilinx ISE, ModelSIM, Hspice, LT-Spice, ORCAD

Programming Language : VerilogHDL, VHDL,C, Assembly Language (MCS51, PIC 16F877A, & ADSP 2191),Pspice.

FPGA/CPLD/Microcontroller: Xilinx FPGAs (Spartan3, Spartan3E, Virtex4)

Area of Interest

- Micro& Nano Electronics Semiconductor Devices.
- Digital and Analog Integrated Circuit Design
- Digital System Design.
- VLSI Technology and Design
- Embedded System Design

Ph.D Thesis Work:

Title:- Device Design Considerations and Performance Analysis of Multiple Gate Junctionless Transistor.

M. Tech Dissertation Work:-

Title:- **Use Of TCAD Tool for The Fabrication of Nano-Scale Bulk MOSFET and its Performance Investigation**

Project Associate at IIT-M (2006-2007):-

Centre for Industrial Consultancy and Sponsored Research(IC & SR), IIT-Madras.
Title: Sparse Area Communication System (SACS), Design of Satellite System.

- Tested one of the Remote Terminal (RT) at ISRO (SAC) to pass voice and data between RT which was installed at ISRO and the Hub at IIT-M tested successfully with data rate at 128kbps.
- RF Testing of Satellite System when using signal generator and to compare it with actual transmitted signal through Hub terminal.
- Testing of FEC Card for the vocoder to boot properly and bit error rate (BER) testing for better constellation of QPSK signal
- Work on SPORTS & DMA configuration of Analog Processors ADSP (2191) on Modem which is the integral part of Hub and Remote terminal.
- Played a major role in Research & Development and for single channel as well as for Multi Channel Tx and Rx for Remote and Hub.

Place: New Delhi Dr. S. Intekhab Amin
Date: 10/09/2024