Curriculum Vitae

1.	Name:	Dr. Md. Waseem Akram
2.	Designation:	Assistant Professor
3.	Date of Birth:	20th September 1985
4.	Qualification:	PhD (IIT Kanpur)
5.	Teaching/Research Experience:	3 Years
6.	Office Address:	Department of Electronics & Communication Engineering, Faculty of Engineering & Technology, Jamia Millia Islamia, Jamia Nagar, New Delhi-110025
7.	Telephone (Direct):	09760984755
8.	Email:	makram1@jmi.ac.in, akrammw@gmail.com
9.	Research Areas:	a. Modeling and Simulation of Semiconductor Devices (Such as, Tunnel FETs, Junctionless FETs, FinFETs, GAA-FETs etc.), Nanoelectronics, Atomistic Simulation. b. Organic Electronic Devices (Especially Organic LED, Organic Solar Cells, Organic TFTs). c. Robust design of semiconductor devices and memories. d. Low Power VLSI Design, Ultra Low Power Design, Digital and Analog VLSI Circuits & Systems. e. Renewable energy, Energy harvesting, Spintronics, Embedded Systems.

10. Teaching/Administrative Experience

1. Presently working as an Assistant Professor in the Dept. of ECE, Faculty of Engg. & Technology, JMI, New Delhi, joined the Institute on 30th August 2016.
2. Worked as an Asst. Prof. in the Dept. of ECE, NIT Patna from 9th July 2015 to 29th August 2016.
3. Worked as a Guest Faculty in the Electronics Engineering Department of ZHCET, Aligarh Muslim University from July 2010 to November 2010.

11. Academic Qualifications

1. **Ph.D.** with a specialization Microelectronics, VLSI, and Display Technology in the **Department of Electrical Engineering, IIT Kanpur**, obtained **CGPA of 7.5** in the year June 2015.
2. **M.Tech** (Electronic Circuits & Systems Design) from **Aligarh Muslim University**, **Aligarh**, **obtained 73.41%** in the year 2010.
3. **B.Tech** (Electronics & Tele-Communication) from **National Institute of Science and Technology, Orissa (UGC NAAC accredits NIST with 'A' grade with highest CGPA of 3.22)**, **obtained CGPA of 7.78** in the year 2008.
4. **12th Standard** from BIEC (A N College, Patna, and Bihar), **obtained 52.33%** marks in the year 2002.
5. **10th Standard** from BSEB (High School Salmari, Salmari, Bihar), **obtained 78.71%** marks in the year 2000.
6. **Certificate of Proficiency in Arabic Language** for the duration of one year at Aligarh Muslim University, Aligarh in the year 2009.
7. **Certificate of Proficiency in Japanese Language** for the duration of one year at National Institute of Science and Technology, Berhampur, Orissa in the year 2006.

12. Training Undergone

1. Precipitated in the 1-month "Orientation Programme" held at UGC-Human Resource Development Center, JMI, New Delhi during Feb. 20-March 28, 2018.
2. Precipitated in the 1-week "Induction Programme" held at UGC-Human Resource Development Center, JMI, New Delhi during 16-22 December 2016.
3. Precipitated in the Summer Internship Programme on Microcontroller Based Embedded System Design at TI Center for Embedded Product Design, NSIT Delhi during 6th June-1st July 2016.
4. Participated in the 1-month summer training on "Electronic Design Automation software Tools for VLSI/ASIC Design" held at NIST, Berhampur in the year 2007.
5. Participated in the 1-month summer training on "Introduction to Oracle 9i: SQL" held at National Institute of Science and Technology (NIST), Berhampur in the year 2005.

13. Projects/Thesis Undertaken

1. **Ph.D. Thesis:** "Junctionless Tunnel FET", under the supervision of Dr. Bahniman Ghosh in the Electrical Engineering Department at IIT Kanpur.

2. **M. Tech Dissertation:** "Variability aware design of an adder" under the supervision of Prof. Mohd. Hasan, Department of Electronics Engineering, AMU, Aligarh.
3. **M. Tech. Project:** "Variability analysis of low power full adder circuits at 45nm technology node" under the supervision of Prof. Mohd. Hasan, Department of Electronics Engineering, AMU, Aligarh.
4. **B. Tech Project: "**A Radio-Coverage Prediction Model in Wireless Communication Systems Based on Physical Optics and the Physical Theory of Diffraction using MATLAB", under the guidance of Dr. Trilochan Panigrahi, NIST, Orissa.

14. Courses Credited/Audited during the M.Tech. and PhD Program

- Microelectronics, Electronics Circuits, Advanced Microprocessor Systems & Design, Advanced Analog IC Design, Active Monolithic Filters, VLSI System Design, Digital System Design Using HDL, Low Power VLSI Design, Semiconductor Memories, Solid State Device, Integrated Circuit Fabrication Technology, Organic Electronics, Analog VLSI Design, Semiconductor Device and Modeling, Compact Modeling.

15. Technical Skills

- **Languages** : C, C++, VHDL, Verilog-HDL, Assembly language 8085.
- **Database** : Operational knowledge of ORACLE 9i.
- **Application Software's** : PSPICE, HSPICE, Xilinx ISE-9.1i, Tanner Tools, Mentor Graphics, MATLAB, Synopsys TCAD (Taurus Medici, Sentaurus Device), Silvaco TCAD (Atlas, Athena).

16. Awards and Recognition

- My biography has been selected in the **Marquis Who's Who in the World 2015 (32nd Edition), 36913566**
- **Reviewer,** Journal of Engineering Science and Technology (JESTEC) (Malaysian Journal)
- **Reviewer**, Superlattices and Microstructures (Elsevier, U.K.)
- **Reviewer**, IEEE Electron Device Letters (IEEE, U.S.A.)
- **Reviewer**, International Journal of Electronics (Taylor & Francis, U.K.)
- **Reviewer**, IEEE Transactions on Device and Materials Reliability (IEEE, U.S.A.)
- **Reviewer**, IETE Journal of Research (IETE, India)
- **Reviewer**, IEEE Electron Device Society (IEEE, U.S.A.)
- **Reviewer**, International Journal of Nanoscience (World Scientific)
- **Received Scholarship** from the Ministry of Human Resource Development, Govt. of India for pursuing Ph.D. program in Engineering from 2011 to 2015.
- **Received Scholarship** from the Ministry of Human Resource Development, Govt. of India for pursuing Master program in Engineering during 2008-2010.

17. Achievements

- Graduate Aptitude Test in Engineering (**GATE**) qualified in ECE branch on 2007, 2008.
- Oracle Certified Associate (**OCA)** Certified.
- **District Third** Position in **10th Standard** Bihar School Examination Board.

18. Professional Memberships

- Member, IEEE, 92619540
- Associate Member (Lifetime) of IETE, AM 236632
- Life Member of ISTE, LM 96683

19. Details of Academic Work at J.M.I., New Delhi

Current/Past Administrative Responsibilities at JMI:

1. Coordinator, B.Tech. Major Project during 2016-2017
2. Coordinator, B.Tech. Seminar during 2016-2017
3. Coordinator, M.Tech. Minor Project during 2017-2018
4. Coordinator, M.Tech. Seminar during 2017-2018
5. DRC Committee Member 2017-2018
6. Coordinator Departmental Magazine 2017-2018
7. Coordinator NBA, Dept. of ECE

Expert Lectures/Seminar, Workshops, short-term courses Arranged/Organized at JMI

1. Dept. of Electronics and communication engineering, JMI, New Delhi in collaboration with Integrated Microsystem, Shivaji Nagar, Gurgaon-122001, and India conducted a Seminar on **"Atomistix toolkit (ATK) & Virtual NanoLab (VNL) Software from QuantumWise"** on 3rd April 2017. **(Programme Coordinator)**

2. Department of Electronics and Communication Engineering organized an Expert Lecture on **"DBMS and its Applications"** given by Mr. M. Y. Ansari, Scientist F, DESIDOC, DRDO, Metcalfe House, Delhi held on 24th April 2017**.(Organizing Committee Member)**

3. Dept. of Electronics and communication engineering, JMI, New Delhi in collaboration with APTRON Solutions Pvt. Ltd., Noida organized an **"On Campus Project Based Training on Robotics"** on 25th April 2017. **(Organizing Committee Member)**

4. Dept. of Electronics & Communication Engineering, JMI, New Delhi in collaboration with ACE Engineering Academy, New Delhi conducted a one day seminar on the topic **"How to Crack IES, GATE and PSUs in first attempt"** held on 7th September 2017. **(Programme Coordinator)**

5. Dept. of Electronics & Communication Engineering, JMI, New Delhi in collaboration with the Cadre Design Systems, Ghaziabad, India organized a one day seminar on the topic **"TCAD simulation of Nanoscale Devices, Circuits and their reliability issues"** held on 14th September 2017. **(Programme Coordinator)**

PhD Students Guiding- 05

Name of the PhD Scholar	Title of PhD Thesis	Department/Institute Name	Supervisor/ Co-Supervisor
Dipak Kumar Singh	Performance Evaluation of Novel Nanoelectronics Devices for Low Power and High Speed Application	Dept. of ECE, NIT Patna	Co-Supervisor
Zeba Mustaqueem	Design and Analysis of Memristor based Analog and Digital Circuits	Dept. of EE, JMI, New Delhi	Co-Supervisor
Zainab Haseeb	Realization of immittances using modern active building blocks and their applications	Dept. of ECE, JMI, New Delhi	Co-Supervisor
Mayank Kumar	Realization of Fractional order Analog Signal Processing/ Signal Generation Circuits	Dept. of ECE, JMI, New Delhi	Co-Supervisor
Satya Prakash Singh	Nanoelectronics	Dept. of ECE, JMI, New Delhi	Supervisor

Courses taught/teaching at Postgraduate and Undergraduate levels:

Advanced Analog Signal Processing, Advanced Digital Signal Processing, Digital Circuit and Systems, Digital Signal Processing, Signals and Systems.

Lab Conducted/Conducting:

Advanced Analog Processing Lab, Circuit Simulation Lab, Digital Signal Processing Lab, Digital Circuits Lab, Advanced Digital Signal Processing Lab.

20. Details of Academic Work at NIT Patna and AMU Aligarh

Administrative Responsibility at NIT Patna

- Prof In-Charge of the Department Examination Section.
- Prof In-Charge of the Semiconductor Devices Lab.
- Prof In-Charge of the VLSI and Embedded System Lab.
- Prof In-Charge of the Project Lab.

Extra-Curricular Activities at NIT Patna

- Coordinator of the "VLSI and Embedded System" Faculty Development Training Program under the Electronics ICT Academy held on 9th-18th Dec. 2015 at Dept. of ECE, NIT Patna.
- Coordinator of the one Day Technical Seminar on the topic "Semiconductor Characterization and Material Measurement" held on 17th March 2016 at Dept. of ECE, NIT Patna.
- Coordinator of the one day Technical Seminar on the topic "Infrastructure Development for Embedded Systems Workshop" held on 30th March 2016 at Dept. of ECE, NIT Patna.
- Coordinator of the 4-week Faculty Development Training Program under the Electronics ICT Academy on the topic "Microcontroller based Embedded System Design" held on 11th July to 2nd August 2016 at Dept. of ECE, NIT Patna.
- Invited Guest Expert in the Annual Tech Fest at NIT Patna held on 22th Jan. to 27th 2016.
- Participated in the SMDP project review committee meeting at IIT Delhi on 12th February 2016.
- Participated in the Electronics and ICT Academy project review committee meeting held at C-DAC Hyderabad on 20th February 2016.
- Organizing Committee Member of the Course "Analog Electronic Circuits" Faculty Development Training Program under the Electronics ICT Academy at NIT Patna held on 19th-28th Feb. 2016.

Invited Lecture Given/ Lab Conducted

- Lecture given on the topic "Junctionless Field Effect Transistor (JLFET): An Attractive Device for Future Technology Node", during the Faculty Development Training Program under Electronics and ICT Academy at NIT Patna on 10th of December 2015.
- Conducted "Analog Electronics Circuit" Lab. using Micro-Cap 10.0 Software during the Faculty Development Training Program under Electronics and ICT Academy at NIT Patna on 19th - 28th February 2016.

Subjects Taught at NIT Patna

- VLSI Design
- Network Analysis and Synthesis (Combined)
- VLSI Fabrication Technology (Combined)

Lab Conducted at NIT Patna

- Elements of Electronics Lab
- Semiconductor Devices Lab
- VLSI Design Lab

Supervised at NIT Patna

- 2 B.Tech. Students

Subjects Taught at AMU

- Microprocessors and Microcontroller (3rd year Undergraduate Students)
- Programming in C (1st year Undergraduate Students)

Lab Conducted at AMU

- Electronic Circuits & Systems Lab (3rd year Undergraduate Students)
- Digital System Design Using Verilog-HDL (3rd year Undergraduate Students)

21. Research Project

1. Start-Up Research Grant: UGC Faculty Research Promotion Scheme **(ongoing)**

22. List of Published/Accepted/Communicated Journal Papers

1. Mayank Kumar; Dinesh Prasad; **Md. Waseem Akram**, Current mode fractional order filters using VDTAs with Grounded capacitors, Accepted for publication in the journal "International Journal of Electronics and Telecommunications".
2. Dinesh Prasad, Zainab Haseeb, Mainuddin, and **Md. W. Akram**, Realization of resistorless floating inductor using modified CDTA, Indian Journal of Pure & Applied Physics (IJPAP), vol. 57 (1), January 2019, pp. 29-32.
3. Mayank Kumar; Dinesh Prasad; **Md. Waseem Akram** , "Current mode fractional order low pass and high pass filter using VDTAs", Indian Journal of Pure & Applied Physics (IJPAP), Vol.56 (07), July 2018, pp. 533-537.
4. Mohd Adil RaushaN, Naushad Alam, **Mohd Waseem Akram**, and Mohd Jawaid Siddiqui, "Impact of asymmetric dual-k spacers on tunnel field effect transistors", Journal of Computational Electronics, June 2018, Volume 17, Issue 2, pp 756–765
5. Partha Mondal, Bahniman Ghosh, Punyasloka Bal, **M. W. Akram**, Akshaykumar Salimath, "Effects of non-uniform doping on junctionless transistor", **Applied Physics A (Material Science and Processing)**, pp. 1-6, February 2015**. (SCI Impact Factor: 1.694)**
6. Uzma Khan, Bahniman Ghosh, **M. W. Akram**, Akshaykumar Salimath, "A comparative study of SELBOX-JLT and SOI-JLT", **Applied Physics A (Material Science and**

Processing), August 2014, DOI 10.1007/s00339-014-8661-3. **(SCI Impact Factor: 1.694)**

7. **M. W. Akram**, Bahniman Ghosh, "Junctionless silicon-nanowire gate-all-around tunnel field effect transistor", **Journal of Low Power Electronics**, vol. 10, pp. 286-292, 2014. **(Scopus Impact Factor: 0.485)**
8. Bahniman Ghosh, Partha Mondal, **M. W. Akram**, and Punyasloka Bal, "Impact of High-κ Spacer on Junctionless Transistor in Sub-threshold regime", **Journal of Low Power Electronics**, vol. 10, pp. 293-296, 2014. **(Scopus Impact Factor: 0.485)**
9. Bahniman Ghosh, Neelam Surana, **M. W. Akram**, "Differentially graded junctionless transistor", **Journal of Electron Devices**, Vol. 19, 2014, pp. 1680-1685
10. Bahniman Ghosh and **Mohammad Waseem Akram**, "Junctionless Tunnel Field Effect Transistor"**, IEEE Electron Device Letters**, vol. 34, no. 5, May 2013, 584-586. **(SCI Imapct Factor: 2.789)**
11. **M. W. Akram**, Bahniman Ghosh, Punyasloka Bal, and Partha Mondal, "P-type double gate junctionless tunnel field effect transistor", **Journal of Semiconductors**, Vol. 35, No. 1, January 2014, 014002-1-7. **(Indexed in Scopus-Elsevier)**
12. **M. W. Akram**, Bahniman Ghosh, "Analog performance of double gate junctionless tunnel field effect transistor", **Journal of Semiconductors,** Vol. 35, No. 7, July 2014. **(Indexed in Scopus-Elsevier)**
13. Punyasloka Bal, Bahniman Ghosh, Partha Mondal, **M. W. Akram**, Ball Mukund Mani Tripathi, "Dual material gate junctionless tunnel field effect transistor", **Journal of Computational Electronics**, Volume 13, Issue 1, pp. 230-234, March 2014. **(SCI Imapct Factor: 1.013)**
14. Punyasloka Bal, **M.W. Akram**, Partha Mondal, Bahniman Ghosh, "Performance estimation of sub-30 nm junctionless tunnel FET (JLTFET)", **Journal of Computational Electronics**, Volume 12, Issue 4, pp. 782-789, December 2013. **(SCI Imapct Factor: 1.013)**
15. Punyasloka Bal, Bahniman Ghosh, Partha Mondal, and **M. W. Akram**, "A laterally graded junctionless transistor", J**ournal of Semiconductors,** Vol. 35, No. 3, pp. 034003, 2014. **(Indexed in Scopus-Elsevier)**
16. Bahniman Ghosh, Punyasloka Bal, Partha Mondal, and **M. W. Akram**, "Device Physics of Germanium-Junctionless Tunnel Field Effect Transistor and an Approach to Optimize Ion/Ioff by Drain Engineering and Work Function Engineering", J**ournal of Low Power Electronics,** Vol. 10, No. 1, March 2014, pp. 92-100(9). **(Scopus Impact Factor: 0.485)**
17. Bahniman Ghosh, Partha Mondal, **M. W. Akram**, Punyasloka Bal, and Akshay Kumar Salimath, "Hetero-Gate-dielectric double gate Junctionless Transistor (HGJLT) with reduced Band-to-Band Tunneling effects in Subthreshold Regime", **Journal of Semiconductors,** Vol. 35, No. 6, June 2014. **(Indexed in Scopus-Elsevier)**
18. Uzma Khan, Bahniman Ghosh, and **M. W. Akram**, "Effect of Self Heating on Selective Buried Oxide and Silicon on Insulator Based Junctionless Transistors", **Journal of Low Power Electronics**, Vol. 9, 1–7, 2013. **(Scopus Impact Factor: 0.485)**
19. Bahniman Ghosh, Uzma Khan, Ball Mukund Mani Tripathi, and **M. W. Akram, "**Ultrathin Compound Semiconductor in Bulk Planar Junctionless Transistor for High-Performance Nanoscale Transistors", **Journal of Low Power Electronics,** Vol. 9, 1–6, 2013. **(Scopus Impact Factor: 0.485)**

20. Bahniman Ghosh, Neelam Surana, **M. W. Akram**, and Ball Mukund Mani Tripathi, "$In_{0.25}Ga_{0.75}As$ Channel Double Gate Junctionless Transistor", **Journal of Low Power Electronics,** Vol. 10, No. 1, pp. 101-106, 2014. **(Scopus Impact Factor: 0.485)**
21. Bahniman Ghosh, Rahul Mishra, **M. W. Akram**, "Device and Circuit Performance Evaluation of Extended Channel SiGe Double Gate Tunnel FETs", **International Journal of Nano Devices, Sensors and Systems (IJ-Nano)**, Vol. 1, No. 1, May 2012, pp. 1-11.
22. Rahul Mishra, **M. W. Akram**, and Bahniman Ghosh, "NEGF analysis of double gate SiGe and GaAs Tunnel FETs"**, International Journal of Electronics, Computer and Communications Technologies** 2012, Vol. 2 (2), 24-26.
23. B. Pavan Kumar, **M. W. Akram**, Bahniman Ghosh, Joseph John, "Drift Effects in HgCdTe Detectors", **Journal of Engineering Science and Technology**, Vol. 8, No. 4 (2013) 472 – 481**. (Indexed in Scopus-Elsevier)**
24. Dharmendra Hiranandani, Akshaykumar Salimath, Bhupesh Bishnoi, Vikas Nandal, **M. W. Akram** et al., "Magnon scattering in single and bilayer graphene intercalates", **Journal of Applied Physics** 112, 114308 (2012). **(SCI Imapct Factor: 2.210)**
25. Ashish Kumar, **M. W. Akram**, and Bahniman Ghosh, "Semiclassical Monte Carlo simulation studies of spin dephasing in InP and InSb nanowires", **AIP Advances** 2, 012165 (2012); doi: 10.1063/1.3694892. **(SCI Imapct Factor: 1.349)**
26. Ashish Kumar, **Md. Waseem Akram**, Satya Gopal Dinda, and Bahniman Ghosh, "Spin dephasing in silicon germanium (Si1xGex) nanowires", **J. Appl. Phys.** 110, 113720 (2011); doi: 10.1063/1.3666022. **(SCI Imapct Factor: 2.210)**
27. Ashish Kumar, **M. W. Akram**, and Bahniman Ghosh, "Spin Relaxation in Germanium Nanowires", **International Scholarly Research Network (ISRN) Nanomaterials**, Volume 2012, Article ID 207043, 7 pages, doi:10.5402/2012/207043. **(Hindawi Publication)**
28. Ashish Kumar, **Md. Waseem Akram**, Satya Gopal Dinda, and Bahniman Ghosh, "Spin Relaxation in Silicon Nanowires", **Journal of Computational and Theoretical Nanoscience,** Vol. 9, 1–6, 2012. **(SCI Imapct Factor: 0.66)**
29. Akshaykumar Salimath, Kapil Jha, **M. W. Akram**, B. B. Himangshu, H. S. Prasad, and Bahniman Ghosh, "Sensitivity of Spin Relaxation to Width Variations in InP Nanowires", **J. Spintron. Magn. Nanomater.** 1, 151-156 (2012).
30. Soumitra Shukla, Bahniman Ghosh, and **Mohammad Waseem Akram**, "1-Bit Full Adder Implementation Using Single Spin Logic Paradigm", SPIN**, World Scientific Publishing Company**, Vol. 2, No. 2 (2012) 1250012 (9 pages). **(SCI Imapct Factor: 0.909)**
31. Bahniman Ghosh, Bhuktare Swapnil, Priyesh Surana, **M. W. Akram**, "Current Voltage Characteristics Modelling of polycrystalline CdTe-CdS solar cells for different grain-sizes of CdTe", **International journal of Nanoelectronics and Materials** 6 (2013) 37-44. **(Indexed in Scopus-Elsevier)**
32. Bahniman Ghosh, Diptarka Chakravarty, and **M. W. Akram**, "Optimization of Digital Circuits using Quantum Ant colony Algorithm", **AJEEE: Australian Journal of Electrical & Electronics Engineering,** Vol. 11, No. 1, 2014, pp. 17-21.
33. Bahniman Ghosh, Ankita Agarwal, and **M. W. Akram**, "An Efficient Quantum-Dot Cellular Automata Multi-Bit Adder Design Using 5-Input Majority Gate", **Quantum Matter,** Vol. 3, No. 5, October 2014, pp. 448-453(6).

34. **M. W. Akram**, Bahniman Ghosh, Punyasloka Bal, and Partha Mondal, "Investigation of high performance 10-nm double gate junctionless tunnel field effect transistor", Quantum Matter, Volume 4, Number 6, December 2015, pp. 549-554(6).
35. Ankita Agarwal, Bahniman Ghosh, and **M. W. Akram**, "Quantum Dot Cellular Automata Read Only Memory using Novel Seven-Input Complex Gate**",** Quantum Matter, Volume 4, Number 2, April 2015, pp. 156-162(7).
36. Navhakar Rahul Shivaji, **Mohammad Waseem Akram**, Bahniman Ghosh, "Design of 6-Bit Two-step Flash ADC for High Speed and Low Power Applications", **Journal of Electronic Design Technology**, Volume 3, Issue 1, April 2012, Pages 15-25.
37. Aminul Islam, **M. W. Akram**, Mohd. Hasan, "Energy Efficient and Process Tolerant Full Adder in Technologies Beyond CMOS", **Int. J. on Recent Trends in Engineering & Technology**, Vol. 05, No. 1, May 2011.

23. <u>List of Published/Accepted/Communicated Conference Papers:</u>

1. Dipak Kumar Singh, Puli Kishore Kumar, **M.W. Akram**, Investigation of Planar and Double-Gate Junctionless Transistors with Non-Uniform Doping, 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), 2-4 Nov. 2018.
2. Zeba Mustaqueem, A. Q. Ansari, and **M. W. Akram**, "Design and Analysis of Efficient Memristor Based Sub-Threshold SRAM Cell", Accepted for presentation in the conference "International Conference on Advanced Materials (ICAM-2019)" scheduled during 6-7th March 2019.
3. Dipak Kumar Singh, Priyanka Mondal, and **M. W. Akram**, "Bulk Multigate Junctionless Transistor (BMGJLT) with Non-uniform Doping Profile: An Attractive Device for Scaling", Accepted for presentation in the conference "International Conference on Advanced Materials (ICAM-2019)" scheduled during 6-7th March 2019.
4. A. Islam, F. Aziz, M. Hasan, **M. W. Akram**, "Analysis of Impact of Device Parameters Fluctuation on SRAM Cell for Process-Tolerant Cache Architecture," **in Proceedings of International Conference on Advances in Electrical & Electronics Engineering (ICAEEE-2011)**, Moradabad, Uttar Pradesh, India, 25-26 Feb., 2011.
5. A. Islam, **M. W. Akram**, M. Hasan, "Variability Immune FinFET-Based Full Adder Design in Subthreshold Region," **in Proceedings of International Conference on Devices and Communications 11 (ICDeCom 11)**, BIT, Mesra, Ranchi, Jharkhand, India, February 24-25, 2011.
6. A. Islam, **M. W. Akram**, M. Hasan, "Variation Resilient Subthreshold Full Adder Cell," **in Proceedings of National Conference on Information and Communication Technology - 2010 (NCICT - 10)**, Nagpur, Maharashtra, India, pp. 27-32, December 23-25, 2010.
7. A. Islam, **M. W. Akram**, Ale Imran, Mohd. Hasan, "Energy Efficient and Process Tolerant Full Adder Design in Near Threshold Region using FinFET, "**IEEE International Symposium on Electronic System Design (ISED-2010)**, Bhubaneswar, India, 20-22 Dec., 2010.

8. S. D. Pable, **M. W. Akram**, M. Hasan, A. Islam, "Variability aware interconnect driver design for subthreshold circuits," **International Conference on Communication, Computers and Devices (ICCCD-2010), IIT, Kharagpur**, INDIA 10-12 Dec. 2010.
9. A. Islam, **M. W. Akram**, M. Hasan, S. D. Pable, "Robust 1-Bit Full Adder Design using FinFET at 32 nm Technology Node," **International Conference on Communication, Computers and Devices (ICCCD-2010)**, IIT, Kharagpur, India, 10-12 Dec. 2010.
10. A. Imran, M. Hasan, **M. W. Akram**, "Design of High frequency low power CMOS Dual-Output Current Conveyor at 32nm technology node," **International Conference on Advances in Recent Technologies in Communication & Computing, ARTCom 2010**, DOI: 10.1109/ARTCom.2010.85, 2010, pp.200-203,16-17 Oct 2010.
11. A. Islam, **M. W. Akram**, S. D. Pable, M. Hasan, "Design and Analysis of Robust Dual Threshold CMOS Full Adder Circuit in 32nm Technology**," IEEE International Conference on Advances in Recent Technologies in Communication & Computing, ARTCom 2010**, pp. 418-420, 16-17 Oct 2010.
12. A. Islam, **M. W. Akram**, S. D. Pable, Mohd. Hasan, "Statistical Data Stability and Leakage Evaluation of SRAM Cell in Sub-45nm Technology," **IEEE International Conference on Advances in Communication, Network, and Computing CNC 2010**, pp. 149-152, 4-5 Oct 2010.
13. A. Imran, M. Hasan, S. D. Pable, **M. W. Akram**, "High Performance Optimized CNFET based Current Conveyor at 32nm technology node**," International Conference on Computer and Communication Technology (ICCCT-2010), 17-19 Sept., 2010, Allahabad**, DOI: 10.1109/ICCCT.2010.5640522,pp.324-329, India,2010.
14. A. Islam, **M. W. Akram**, S. D. Pable, Mohd. Hasan, "Design of a Novel CNTFET-Based 1-Bit Full Adder in Deep Submicron Technology," **14th VLSI Design and Test Symposium, VDAT 2010**, July 7-9, 2010.
15. S. D. Pable, A. Islam, **M. W. Akram**, M. Hasan, "Design of Robust Subthreshold Circuits," **14th VLSI Design and Test Symposium, VDAT2010,** July 7-9, 2010.

24. <u>Workshops, Conferences, and Seminars Attended</u>

1. Attended a TEQIP-II Sponsored 1 day workshop on **"Analog IC Design using SCL CMOS Technology"** organized by Dept. of Electronics Engineering, Aligarh Muslim University, and Aligarh held on 9th October 2016.
2. Attended 3 days' **Familiarization Workshop on Nanofabrication Technologies** held at IIT Bombay during May 25-27, 2016.
3. Attended a 5 days TEQIP sponsored short term course on **'Microwave Wireless Components for Transmitter and Receiver Systems'** held on 30th May to 3rd June 2016 organized by Dept. of ECE, NIT Patna.
4. Attended a 10 days Faculty Development Training Program under the Electronics ICT Academy NIT Patna on **"Analog Electronic Circuits"** at Dept. of ECE, NIT Patna held on 19th -28th Feb. 2016.
5. Attended a 1 day workshop on **"CMOS Design with HiSIM MOS model"** organized by Dept. of ECE, NIT Durgapur held on 10th March 2016.
6. Attended a Seminar on **"CMOS Circuit Designs for Biomedical and Memory Applications"** organized by Dept. of Electrical Engg, IIT Kanpur held on 14th May, 2015.

7. Attended a Seminar on **"Advanced Radio Frequency (RF) and CMOS Devices: Modeling, Characterization and Fabrication"** organized by Dept. of Electrical Engg, IIT Kanpur held on 13th May, 2015.
8. Attended a Seminar on **"Low power neuromorphic computing with Tunneling Field Effect transistors (TFETs)"** organized by Dept. of Electrical Engg, IIT Kanpur held on 23rd April, 2015.
9. Attended a half day Technology Workshop on **"MATLAB and Robotics"**, conducted by Mathworks, Bangalore, organized by Computer Centre, IIT Kanpur, held on 15th March 2015.
10. Attended a half day Technology Workshop on **"MATLAB and High Performance Computing",** conducted by Mathworks, Bangalore, organized by Computer Centre, IIT Kanpur, held on 14th March 2015.
11. Attended a Seminar on **"Facilities at Centre for Nano Science and Engineering, IISc Bangalore"** organized by Dept. of Electrical Engg, IIT Kanpur held on 16th Jan. 2015.
12. Attended a Seminar on **"Development of ultra-thin dielectric for organic thin-film transistors"** organized by Dept. of Electrical Engg, IIT Kanpur held on 6th Jan. 2015.
13. Attended a Seminar on **"TCAD Assisted FinFET Device Design"** organized by Dept. of Electrical Engg, IIT Kanpur held on 26th December 2014.
14. Attended a Seminar on **"How to use atomistic simulator for electron device research"** organized by Dept. of Electrical Engg, IIT Kanpur held on 29th September 2014.
15. Attended a Seminar on **"RF CMOS circuits and roadmap for 5G technologies"** organized by Dept. of Electrical Engg, IIT Kanpur held on 4th September 2014.
16. Attended a two day's Indo-US workshop on **"Organic Solar Cells"** organized by Dept. of Electrical Engg, IIT Kanpur held on 20th-21th March 2014.
17. Attended a Seminar on **"TCAD Enabled Sub-10nm-FinFET Device Design"** organized by Dept. of Electrical Engg, IIT Kanpur held on 14th March 2014.
18. Attended a three day Technology Workshop on **"MOSFET compact modeling"** conducted by IBM's Semiconductor Research & Development Center (SRDC) held on 5-7 April, 2013 at IIT Kanpur.
19. Attended a Seminar on **"Polymer and Printable Transistors: Recent Advances"** organized by Dept. of Electrical Engg, IIT Kanpur held on 14th March 2013.
20. Attended a Seminar on **"MBE grown Quantum-Dot UV Light Emitting Diodes with Tunnel-injection and Polarization-engineering"** organized by Dept. of Electrical Engg, IIT Kanpur held on 5th Jan. 2013.
21. Attended a half day workshop on **"Recent Advances on Indian Space Technology"** conducted by ISRO-IITK-Space Technology Cell held on 6 November 2012,IIT Kanpur.
22. Attended a Seminar on **"Edge effects in Graphene nanoribbon MOSFETs: an atomistic simulation study"** organized by Dept. of Electrical Engg, IIT Kanpur held on 31th Oct 2012.
23. Attended a half day Technology Workshop on **"Future CMOS Technology"** conducted by IBM Systems and Technology Labs (ISTL) held on 30th Oct, 2012 at IIT Kanpur.
24. Attended a three day Technology Workshop entitled **"XVI International Workshop on the Physics of Semiconductor Devices (IWPSD 2011)"** organized by the Indian Institute of Technology Kanpur and Semiconductor Society of India at IIT Kanpur on December 19-22, 2011.
25. Participated in two day's National Symposium on **"Developments in Instrumentation and**

control engineering" Organized by Department of Electrical Engineering, held at AMU, Aligarh, on 27-28 March, 2010.

26. Participated in one day Workshop on **"Recent Trends in VLSI Design and Technology (VDT-2010)"** Organized by Department of Electronics Engineering, held at AMU, Aligarh, on 20th March, 2010.
27. Participated in 3 **day's "International Conference on Multimedia, Signal Processing, and Communication Technologies"** Organized by Department of Electronics Engineering, held at AMU, Aligarh, on 14th -16th March, 2009.
28. Participated in one day seminar on **"VLSI design using Tanner Tools"** organized by Tanner EDA, USA, held at NIST, Berhampur, Orissa, on 5th November 2007.
29. Participated in one day Workshop on **"Bioinformatics"** Organized by NIST, Berhampur, Orissa, on 4th March 2006.

Dr. M. W. Akram

Date: 25/1/2019