HAFSA NIGAR

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+91-9354185591

New Delhi, INDIA

ACCOMPLISHMENTS

- Qualified Graduate aptitude test in Engineering (GATE) in 2016.
- Merit Scholarships in school and college.
- Received best paper presentation award in JTA conference, JMI, February 2020.
- Won the interfaculty badminton championship trophy.
- Won interschool debate competitions.

LANGUAGE

English

Urdu

Hindi

Objective

To pursue a challenging career path and join a forward-thinking institution that lets me use and improve my knowledge and skills. My goal is to achieve the highest level of success in research and academics.

WORK EXPERIENCE

August 2024- Till date

- **Assistant professor (Contractual)**, Department of Electronics and Communications Engineering, Faculty of Engg and Tech., JMI, New Delhi, India.

July 2018- June 2023

- **Guest Lecturer**, Electronics and Communications Engineering, University Polytechnic, JMI, New Delhi, India.

Sept 2012 - May 2015

- **Guest Lecturer**, Electronics and Communications Engineering, University Polytechnic, JMI, New Delhi, India.

EDUCATION

- **[2016-2023]** Ph.D. in Electronics and Communications Engineering from Jamia Millia Islamia, New Delhi, India.
- **[2010-2012]** Master of Technology in Nanotechnology (CGPA=8.64) from Jamia Millia Islamia, New Delhi, India.
- **[2006-2010]** Bachelor of Technology in Electronics and Communications Engineering (CGPA=9.25) from Jamia Millia Islamia, New Delhi, India.
- **[2006]** Senior secondary school certificate (72 %) from Jamia Millia Islamia, New Delhi, India.
- **[2004]** Secondary school certificate (77 %) from Jamia Millia Islamia, New Delhi, India.

SKILLS AND TOOLS

- Silvaco ATLAS TCAD.
- ORIGIN

PARTICIPATION IN WORKSHOPS/SEMINARS

- 3rd March 2017, attended IEEE workshop on Compact modelling.
- 26th Dec. 2017 to 30th Dec. 2017 Attended GIAN course o"Organic Light Emitting Diodes (OLEDS) for future lighting and Displays", Jamia Millia Islamia, New Delhi, India.
- 4th to 6th July 2024, attended and delivered an expert lecture on Energy Sustainability and Climate Change.

CORRESPONDANCE ADDRESS

D-195, Abul fazl Enclave

Jamia Nagar

New Delhi-110025

INDIA

Research

Research Areas: Power Semiconductor Device Design, Device Reliability and III-V Power Semiconductor Devices.
M.Tech Thesis Title: Simulation Studies of Conventional Overlap and Proposed Underlap Structures on Silicon on Nothing (SON) MOSFET.
Ph.D. Thesis Title: Design and Simulation of High Performance Power Semiconductor Devices.

Publications

Patents

1. Hafsa Nigar and Sajad A. Loan "Selective Buried Double Gate Power MOSFET: A Method of Manufacturing the Same". Granted . patent no- 538143

2. Hafsa Nigar and Sajad A. Loan "A High Performance Uni-gate Vertical Power MOSFET: A Method of Manufacturing the Same" (Submitted).

SCI listed journals

1. Nigar, Hafsa, Sajad A. Loan, and Abdullah G. Alharbi. "High performance selective buried double gate power MOSFET." Semiconductor Science and Technology 34.5 (2019): 05LT01.

2. Nigar, Hafsa, Hend I. Alkhammash, and Sajad A. Loan. "A Charge Balanced Vertical Power MOSFET with Record High Balliga's Figure of Merit: Design and Investigation." Silicon 14.8 (2022): 3919-3930.

3. Nigar, Hafsa, et al. "AUni-gate vertical power MOSFET with improved figure of Merits: Design and analysis." Alexandria Engineering Journal 67 (2023): 31-38.

4. Nigar, Hafsa, Hend Alkhammash, and Sajad A. Loan. "Charge 'Plasma Based Dual Buried Gates Power MOSFET: Design and Analysis." (2024).

International IEEE Conferences

1. Nigar, Hafsa, and Sajad A. Loan. "Impact of Gate-Drift Overlap on the Figure ofMerits of Dual Buried Gates Power MOSFET." 2019 International Conference on Electrical, Electronics and Computer Engineering (UPCON). IEEE, 2019.

- Place:- NEW DELHI
- Date 6/03/2025

Signature