Thesis Findings

Title of the Thesis: Algorithmic Optimization for Binary Decision Diagram Mapped Logic Circuits

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This thesis focuses on optimizing the various parameters of Binary Decision Diagrams through the use of appropriate optimization techniques. In this thesis, many optimization techniques have been implemented and compared to existing Decision diagram optimization techniques in order to achieve this objective. The following are the thesis's findings:

- The first proposed GA-based approach, the Modified Genetic Algorithm (MGA), employs an enhanced initial population generation strategy in conjunction with enhanced and modified GA operators. Several digital circuits from the LGSynth benchmark suite, as well as digital adder circuits with sizes ranging from 1-bit to 8-bits, have been simulated implementing the proposed MGA implementation. The proposed MGA is compared to a variety of in-built BDD optimization techniques present in various BDD suites. The implementation findings show that the proposed MGA method exhibit improved average node count values.
- A hybrid strategy is employed in the second proposed GA-based approach, which combines the sifting or SIFT algorithm method with the GA-based method. The SIFT method was one of the first BDD variable ordering techniques to acquire widespread acceptance. The proposed hybrid technique aims to incorporate both the algorithm's local and global search features. The proposed work is implemented targeting a reduction in the number of MUXs used in the MUX-based implementation of BDD-mapped digital circuits. When compared to existing methodologies, the proposed work shows a significant reduction in the overall MUX count for several LGSynth91 test circuits.
- The third proposed GA-based study provides an insight into the impact of incorporating the position-based crossover (PX) operator into the conventional

genetic algorithm for node count optimization in BDD-mapped digital adder circuits. The simulation results indicate that the position-based crossover (PX) operator reduces node count more effectively than other approaches, including a GA method that uses the partially-matched crossover (PMX) operator.

- Two Differential Evolution-based techniques for BDD variable ordering targeting node count and longest path length are presented in chapter: DE with Forward Backward Transformation and DE with Relative Position Indexing. This work is compared to a previous BDD optimization work that used the Particle Swarm Optimization (PSO) method. The PSO algorithm has consistently proven to be the most efficient technique among the popular optimization algorithms since its implementation for the optimization of the BDD variable ordering problem. The results of the experiments indicate that both DE techniques have a good reduction in node count for a large number of circuits. Both DE-approaches, however, failed to outperform PSO for LPL optimization.
- A state-of-the-art Spider Monkey Optimization (SMO) technique for BDD-mapped digital circuits is implemented in chapter. This method is also compared to the PSO technique for BDD variable ordering optimization. The work employs node count and LPL as cost functions. Although prior DE-based implementations were successful in node optimization, they were unsuccessful in LPL optimization. However, the proposed SMO-based approach outperforms the PSO technique in terms of both node count and LPL optimization.