REPORT ON PhD RESEARCH FINDINGS

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PhD Topic: "Design and Modeling of Energy Efficient Nanoelectronic Devices at Device & Circuit Level"

PhD Research Findings:

In these five years, the state-of-the-art research related issues with the Tunnel Field Effect Transistor Technology and its potential for future low power device designing were thoroughly investigated through 2D TCAD simulations on Sentuarus TCAD Device Simulator both on circuit as well as device level. Novel designs for performance parameters improvement were proposed. Some critical conclusions derived from the investigations are as follows:

- Leakage reduction using high-k underlap pockets in EHBTFETs is highly sensitive to the bandgap material and can be used as an effective means to improve scalability for future low power designing with smart materials at potentially lower bandgaps.

- While designing pocket-based structures, alignment and shape of pocket implants particularly in TFETs play a significantly important role in determining the design reliability, especially ON current fluctuations and miller capacitance.

- Gate-to-source capacitance in line tunneling designs also plays a significantly important role in determining miller performance unlike conventional point TFETs that are dominated majorly by gate-to-drain capacitance.

- A trade-off exists between line and lateral pockets. Line pockets are ideally suited for narrower widths. Lateral pockets on the other hand, provide boosting at wider pocket widths.

- Material engineering techniques when combined with line tunneling designs can exploit the high vertical tunnel onset of vertical tunneling to provide a mid-way path between leakages due to ITC tolerance, geometrical constraints and provide improved performance.

- However, looking forward to ITRS 2.0 thinking ten years down the line, there still exists a gap to bridge with designs having the potential to perform at VDD as low as 0.1V which requires further improvement in ON current levels and voltage scalability.