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Title of Thesis: "A Scalable Architecture of 3-D Network-on-Chip (NoC)"

Abstract

With the advancement in technology the feature size scales down to deep nanometer regimes, it has enabled the designers to fabricate chips with billions of transistors. The availability of such abundant computational resources on a single chip has made it possible to design chips with multiple computational cores. NoC is recognized as proven solution for growing complicated communication requirements of Multi-Processor System-on-Chip (MPSoC). Shifting from the traditional bus based on-chip communication system to innovative NoC technology is not an easy option, numerous concepts are required to change basically for the designers because of this shift. Introduction of third dimension in the NoC has improved its performance, it gives rise to new research areas and results in emerging 3-D NoC technology, which have reduced latencies compared to 2-D NoC. Research in this area is still open, as response to higher requirements of future applications needing high energy efficiency and high bandwidth communication NoC. This emphasizes the need for energy efficient NoC architecture, and exploration of energy efficient routing algorithms. In this work we have focused on multiple aspects of 3-D NoC. The major contributions of this research work are as follows:

Energy Efficient Routing Algorithms for 3-D NoC Architecture:

To encounter the present and future requirements of electronic systems, integration of 3-D technology is very promising. 3-D Network-on-Chip design augments performance and reduces power consumption with the aid of changing long flat interconnects with smaller vertical links. To attain higher execution speed along with reduced energy consumption optimized routing algorithms are required. A comprehensive assessment of the various routing algorithms used in 3-D NoC at present in literature and industries are specified and an extensive discussion on the problems and challenges for the 3-D NoC is developed. Provided information for choosing routing algorithm so that energy efficiency and the performance of NoC can be anticipated.

Simulation and Performance Evaluation of NoC Architecture for different topologies: Topology can be called as backbone or structure of NoC architecture, and it is one of the main constituent in NoC design. The important parameters which are used for analysis of any NoC are latency, throughput, injection rate and hop count and so on. In this work most popular NoC topologies performance, such as Mesh, Torus, C-mesh, Fat-tree, are evaluated. Simulator is used for reproducing results. From the analysis, it can be determined that the throughput rises linearly with the injection rate however at one point it saturates, furthermore, this is where we get saturation throughput. All the topologies have different injection rate range for a same size network. From these analyses we can state that range of injection rate for C-mesh is very less compared with other topologies and performance of Torus topology is better in comparison with all other topology.

Design and Analysis of Proposed 3-D NoC Routing Algorithm

The ability of routing algorithms to follow path with least number of hops and least latency can provide higher execution speed along with reduced energy consumption. In present work an efficient routing algorithm for 3-D Torus topology architecture is proposed. The proposed algorithm, modified quadrant-based routing algorithm, for 3-D torus NoC architecture is fundamentally based on division of space into four different quadrants and adopting a path which traverses least hops to connect source node to destination node. The synthesis of the proposed algorithm is realized on the Xilinx Virtex-5 XC5VLX110T FPGA. Compared the results obtained from synthesis on FPGA, and it was found that the proposed algorithm has better performance in terms of latency and energy efficiency with other routing algorithms, like, XYZ dimension order routing and quadrant-based algorithm.

Proposed Tree based Scalable Architecture for 3-D NoC

The physical structure of NoC is defined by its topology. Mesh is mostly used because of its simple and regular structure. However, it has many limitations, for example for a larger network sizes, the links requirement is more which requires extra area and power of the chip. Area overhead and power consumption of NoC reduces by reducing the number of links. In this thesis, a scalable binary tree-based topology for 2-D and 3-D NoCs has been proposed. The proposed topology is the combination of binary tree and ring topology for 2-D and 3-D NoC architecture, which drastically reduces the number of links. The average degree of the proposed network is reduced around 40% of the torus whereas the diameter is also reduced significantly, as compared to other topologies, this not only save the area overhead but also, the complexity and cost of router are also reduced.