ABSTRACT

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Title: AREA-EFFICIENT ROUTING IN 3-D NETWORK-ON-CHIP (NOC)

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ABSTRACT - The growing demand of applications in consumer electronics has increased the number of computing resources in single-chip. The applications need many computing resources such as CPU, DSP, and specific Intellectual Property (IP) cores to build a System-on-Chip (SoC). Therefore, interconnection between each other becomes another challenging issue. A typical NoC application consists of multiple storage components (memory cores) and processing elements, such as general-purpose CPUs, specialized cores and embedded hardware connected together over complex communication architecture. The NoC technology has replaced traditional bus architecture with a low-cost point-to-point and packet-based architecture. The advances in integration technologies have enabled the construction of NoC from two dimensional (2-D) to three dimensional (3-D). The 3-D Integrated Circuits (ICs) are able to obtain significant performance benefits over 2-D ICs based on the electrical and mechanical properties resulting from the new geometrical arrangement. The arrangement of 3-D ICs also offers opportunities for new circuit architecture based on the geometric capacity. The emerging 3-D VLSI integration and process technologies allow the new design opportunities in 3-D Network-on-Chip. The 3-D NoC can reduce significant amount of wire length for local and global interconnects. The 3-D IC technology consists of stacking and vertically interconnecting several layers of active circuits. The 3-D NoC application may combine digital, analog, RF circuitry and mixed-signal capability that are critical for providing a complete 3-D IC realization methodology. Without an integrated approach to 3-D IC design, optimizing system cost with the shortest possible turnaround time will be challenging. To reduce the latency and wire length we need an efficient interconnection architecture. Performance of the network is measured in terms of throughput. The throughput and efficiency of interconnection depends on the network parameters for given topology. Therefore, topology of any communication networks has an important role to play for efficient design. The performance of an interconnection architecture depends on degree and diameter. The cost of interconnection architecture can be defined as a value of the *degree* × *diameter*.

In this thesis, we have proposed a Quadrant-XYZ dimension order routing algorithm to route the data in 3-D asymmetric torus topology. The algorithm partitions the geometrical space into quadrants and selects the nearest wrap-around edge to connect the destination node. Thus, the presented algorithm guarantees minimal paths to each destination based on routing regulations.

The complexity of the algorithm is $O(n)$. The 3-D asymmetric torus with Quadrant-XYZ has achieved a maximum operating frequency 750 MHz on Xilinx Vertex-6 programmable device.

In this thesis, we have also examined the architecture of a typical virtual channel router and look at the issues and trade-offs involved in router design. The thesis also presents the design of proposed micro-architecture of 3-D router that reduces circuit complexity and increases the performance. The thesis also provides a detailed discussion on the distribution of traffic in 3-D NoC. The design has passed through Design Rule Check and the area of layout obtained is 3548.64 μm2. The power dissipation is obtained 1.01 mW at the maximum operating frequency of 750 MHz. We have compared the design with existing implementations and found to be optimized.

In 3-D Network-on-Chip a packet need multiple clock cycles to traverse from one router to another because of wires, buffer allocation latency and arbitration cycles. The buffer allocation technique has an important role to play in the design of NoC routers. The buffers are also source for largest leakage power. The present invention introduces a novel architecture for Virtual Channel (VC) Manager to allocate and deallocates multiple virtual channels dynamically according to the traffic pattern. The present invention maximizes throughput by dispensing a variable number of VCs on demand. To reduce the leakage power, a standard clock gating technique is applied to shutdown and power up the clock for individual virtual channels. The present invention has a synchronous FIFO with VC IDs that are pre-written to FIFO which enables dispense of VC ID with zero latency. The FIFO is able to dispense or allocate (Read operation) multiple VC IDs in single clock cycle. A hardware reservation technique is also presented in the invention that provides a reservation policy for allocation of virtual channel. The reservation policy guarantees that one virtual channel would be reserved for every physical channel. The thesis presents invention that relates in general to 3-D Network-on-Chip router and more particularly, to a method of optimizing virtual channel allocation technique using parallel and dynamic approaches. Our invention provides an efficient, fast, and dynamic technique for allocation and de-allocation of virtual channel in 3-D Network-on-Chip.

We have developed a Register Transfer Logic (RTL) level simulation model to evaluate the performance of proposed arbiter for NoC resources. A 640-bit message with uniform random destination data pattern was injected per IP per machine clock cycle. The worst case latency for the proposed design is 35 clock cycles. We have obtained the maximum clock frequency 2.09 GHz for 96(4 x 8 x 3) IP cores connected in a mesh topology. The presented architecture demonstrates its superior functionality in terms of speed and latency as compared with existing implementations. The RTL design is synthesized using Taiwan Semiconductor Manufacturing Corp. (TSMC) Technology.