Name: Faraz Hashmi

Notification No: 584/2025

Notification Date: 18-08-2025

Name of the Supervisor: Prof. (Dr.) M. Nizamuddin

Topic: "Design of Graphene Based Nanoelectronics Circuits for Low Power Applications"

Department: Electronics and Communication Engineering

Findings

In this research, the boundaries of the Si roadmap, Carbon Nanotube Field Effect Transistor (CNTFET) and Graphene Nanoribbon Field Effect Transistor (GNRFET)-based Circuits are being investigated as innovative topologies for next electronics.

First details the design and simulation of a high-gain Triple Cascode Operational Transconductance Amplifier (TCOTA) using CNTFET technology at the 45 nm node. A performance comparison between the proposed CNT-based TCOTA and a conventional CMOS-based TCOTA is presented. The results demonstrate a 73% improvement in DC gain, a 28% higher CMRR, and significantly better figures of merit, confirming CNTFET's superiority for high-gain analog applications.

Second, expanding on the earlier research, investigates the use of GNRFET technology to construct a more energy-efficient and high-performance TCOTA at the 32 nm node. GNRFET-based and two hybrid technology OTAs are best suited for low-power, high-speed Internet of Things (IoT) applications because of their superior Energy-Delay Product (EDP), faster settling time, and higher speed, according to the report.

Third focusses on utilising the special qualities of Armchair GNRs (AGNRs) to maximise the performance of the GNRFET-TCOTA. In comparison to its CMOS equivalent, the optimised pure GNRFET-TCOTA exhibits a noteworthy 8.47x improvement in 3-dB bandwidth and a 5.85x greater slew rate. Furthermore, the computational models for calculating the band structure and density of states (DOS) of AGNRs are presented to underscore the material physics behind the performance gains.

Finally, it wraps up by summarising the main conclusions, which together make CNTFETs and GNRFETs extremely promising technologies that have the potential to transform analogue and mixed-signal circuit design. In order to properly utilize precision-added nanoelectronics, they include resolving fabrication issues for physical validation, improving simulation models for increased precision, and expanding this study to other crucial analogue blocks.